WHAT IS CLAIMED IS:

Sub B6

1. An arrangement for transferring pixel information with respect to pixels arranged in columns and rows of an array of a display device, comprising:

a plurality of semiconductor switches, each having a first terminal, a second terminal and a third terminal;

a first buss coupled to a first plurality of terminals for communicating corresponding signals; and

a plurality of local busses that are separated from one another for communicating corresponding signals, a given local buss having a first buss section coupled to a second plurality of terminals associated with said given local buss and extending in a manner to cross over said first buss and a second buss section extending from said first buss section and having conductors thereof coupled in a local, clustering buss arrangement to the second terminals of switches associated with said given local buss of said plurality of switches, the associated switches having the third terminals thereof coupled to consecutively disposed column conductors, respectively, of said array.

2. An arrangement according to Claim 1 wherein said first plurality of terminals, develop switch control signals and said second plurality of terminals develop picture information signals for said switches to form a demultiplexer for storing the picture information in said pixels of said array.

3. An arrangement according to Claim 1 wherein said associated switches including a plurality of sub-groups of switches, the switches of a given sub-group having the first terminals thereof coupled in common to a corresponding conductor of said first buss and the third terminals thereof being coupled to consecutively disposed column conductors, respectively, of said array.

4. An arrangement according to Claim 1 wherein the conductors of said second buss section of said given local buss are disposed in a vicinity of said switches associated with said given buss and remotely from switches associated with the other local busses of said plurality of local busses to provide buss separation for obtaining the local clustering buss arrangement.

5. An arrangement according to Claim 1 wherein the conductors of said first buss extend along each of said plurality of semiconductor switches to form a global buss arrangement.

Sub D1

6. An arrangement according to Claim 1 wherein said third terminal of each of said semiconductor switches is coupled to an input terminal of a corresponding data line driver.

Sub B7

7. A signal demultiplexer for a display panel, comprising:

a plurality of clusters of switches, each cluster having ordinally numbered switches 1 thru n arranged sequentially, and each switch having respective input, output and control terminals with the control terminals of all switches in each cluster connected to

a common control terminal, and having respective output terminals coupled to successive data lines on said display panel;

a plurality of clusters of data busses, each cluster of data busses having ordinally numbered conductors 1 thru n, the ordinally numbered conductors of respective clusters of data busses being coupled to input terminals of corresponding ordinally numbered switches of a plurality of said clusters of switches;

a control buss including a plurality of conductors, said control buss arranged to crossover said plurality of clusters of data busses; and

connections between ones of said plurality of conductors of said control buss and respective common control terminals of said clusters of switches.

8. A signal demultiplexer for a display panel, comprising:

a plurality of clusters of switches, a given cluster having ordinally numbered switches arranged sequentially, and each switch having respective input, output and control terminals, the output terminals coupled to successive data lines on said display panel;

a cluster of data busses, a given data bus thereof having ordinally numbered conductors arranged sequentially, a given conductor of said given data buss being coupled in common to the input terminal of each switch having the same ordinal number that corresponds to the ordinal number of said given conductor and being included in each cluster of said switches that is associated with said given data bus;

a control buss including a plurality of conductors, said control buss arranged to crossover said clusters of data busses; and

connections between ones of said plurality of conductors of said control buss and respective control terminals of said clusters of switches.

9. A signal demultiplexer according to Claim 8 wherein the control terminals of all the switches in each cluster of switches are connected in common to a corresponding conductor of said control buss.

ADD A2